

What is claimed is:

1. A pixel sensor for providing image sensing under radiation or space environment, comprising:

a readout circuit operating to convert optical image signals to electronic signals, where said readout circuit includes p-type transistors and an n-type photosensitive element; and

a first reset circuit configured to provide a reset level for a pixel output, where said first reset circuit includes at least one p-type transistor,

where said readout circuit and said first reset circuit having said p-type transistors, and said n-type photosensitive element, provide radiation hardness without any radiation protective enclosure.

2. The pixel sensor of claim 1, wherein said p-type transistors are MOSFET p-type transistors.

3. The pixel sensor of claim 1, wherein said n-type photosensitive element is an n-type photodiode.

4. The pixel sensor of claim 3, wherein said n-type photodiode is formed in a square layout design.

1 5. The pixel sensor of claim 3, wherein said n-type
2 photodiode is formed in a circular layout design.

1 6. The pixel sensor of claim 1, further comprising:
2 a p-type substrate on which said n-type photosensitive
3 element is formed.

1 7. The pixel sensor of claim 6, further comprising:
2 a pair of p+ type guard rings formed on said p-type
3 substrate, each of said pair of guard rings formed on either
4 side of said n-type photosensitive element, said pair of
5 guard rings connected to a ground voltage, and operating to
6 substantially reduce a leakage current from said n-type
7 photosensitive element.

1 8. The pixel sensor of claim 6, further comprising:
2 an n-type well provided adjacent to said p-type
3 substrate, said n-type well connected to a supply voltage,
4 and operating to prevent crosstalk between pixels.

1 9. The pixel sensor of claim 1, further comprising:
2 a second reset circuit having a p-type MOSFET
3 transistor coupled to an input of said first reset circuit,
4 said second reset circuit allowing pixel-by-pixel reset
5 operation.

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1 10. A radiation-hard CMOS image sensing device,
 2 comprising:
 3 a p-type substrate;
 4 an n-type photodiode formed on said p-type substrate,
 5 where said n-type photodiode operates to convert an optical
 6 signal to an electrical signal;
 7 a first reset circuit configured to provide a reset
 8 value for said electrical signal, said first reset circuit
 9 including a p-type MOSFET transistor; and
 10 a readout circuit operating to buffer said electrical
 11 signal, said readout circuit including a p-type MOSFET
 12 transistor.

1 11. The device of claim 10, further comprising:
 2 a pair of p+ type guard rings formed on said p-type
 3 substrate, each of said pair of guard rings formed on either
 4 side of said n-type photodiode, said pair of guard rings
 5 connected to a ground voltage, and operating to
 6 substantially reduce a leakage current from said n-type
 7 photodiode.

1 12. The device of claim 11, further comprising:
2 an n-type well provided adjacent to said p-type
3 substrate, said n-type well connected to a supply voltage,
4 and operating to prevent crosstalk between pixels in the
5 CMOS image sensing device.

1 13. The device of claim 10, further comprising:
2 a second reset circuit having a p-type MOSFET
3 transistor coupled to an input of said first reset circuit,
4 said second reset circuit allowing pixel-by-pixel reset
5 operation.

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1 14. A CMOS image sensor system, comprising:
2 an array of active pixel sensors, each pixel sensor of
3 said array including:
4 a pixel readout circuit operating to convert
5 optical image signals to electronic signals, where said
6 pixel readout circuit includes p-type transistors and
7 an n-type photosensitive element, and
8 a first reset circuit configured to provide a
9 reset level for a pixel output, where said first reset
10 circuit includes p-type transistors,
11 where said pixel readout circuit and said first
12 reset circuit having said p-type transistors and said
13 n-type photosensitive element provide radiation
14 hardness without any radiation protective enclosure;
15 a control circuit configured to provide timing and
16 control signals to enable read out of data stored in said
17 array of active pixel sensors; and
18 a column readout circuit operating to receive and
19 process said data stored in said array of active pixel
20 sensors.

1 15. The CMOS image sensor of claim 14, further
2 comprising:
3 a p-type substrate on which said n-type photosensitive
4 element is formed.

1 16. The CMOS image sensor of claim 15, further
2 comprising:

3 a pair of p+ type guard rings formed on said p-type
4 substrate, each of said pair of guard rings formed on either
5 side of said n-type photosensitive element, said pair of
6 guard rings connected to a ground voltage, and operating to
7 substantially reduce a leakage current from said n-type
8 photosensitive element.

1 17. The CMOS image sensor of claim 15, further
2 comprising:

3 an n-type well provided adjacent to said p-type
4 substrate, said n-type well connected to a supply voltage,
5 and operating to prevent crosstalk between pixels.

1 18. The CMOS image sensor of claim 14, further
2 comprising:

3 a second reset circuit having a p-type MOSFET
4 transistor coupled to an input of said first reset circuit,
5 said second reset circuit allowing pixel-by-pixel reset
6 operation.